RAELLA

Reforming the Arithmetic for Efficient, Low-Resolution, and Low-Loss Analog PIM: No Retraining Required!

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Processing In Memory (PIM) Accelerators



Processing In Memory (PIM) Accelerators

Weight matrix stored in crossbar as analog conductance values

Input vector applied to rows as analog temporal values

Analog matrix-vector multiply Charge ~ Conductance × Time

Results appear on columns As analog charge values



Processing In Memory (PIM) Accelerators



The Titanium Law of ADC Energy



Idea: Break computation into smaller pieces Benefit: Smaller result from each piece, J Energy/Convert Tradeoff: More pieces to process, ↑ Converts/MAC



DNN Accuracy















Computations with zero-average weights produce near-zero results











Key Takeaway: Partition computation Digital calculates high-resolution center operations Analog calculates parallel offset operations





Adaptive Weight Slicing: Slice Large-Result Computations







Dynamic Input Slicing: Try Again with Smaller Slices



Reshaping the Distributions of Analog Values



Reshaping the Distributions of Analog Values

1024x reduction in required ADC range



→ Lower Energy ADC (\uparrow Efficiency) and/or → More computations per ADC convert (\uparrow Efficiency, Throughput)

Evaluation

- Full System Simulation comparing accelerators ISAAC and RAELLA
- Both low-accuracy-loss, run DNNs without modification/retraining

Green = Compute

RAELLA gets more compute per unit area, more compute per ADC convert



Evaluation: ISAAC and RAELLA



Evaluation: ISAAC and RAELLA



Key Takeaways

- High ADC energy is a challenge in PIM architectures:
 - Titanium Law can be used to analyze ADC energy tradeoffs
- Reduce ADC energy; make analog computations produce small results:
 - Center+Offset: Shift the mean of each computed distribution to the center of the ADC range
 - Adaptive Weight Slicing: If a computation produces large results, slice it into smaller pieces
 - **Dynamic Input Slicing:** Speculate that results are in-range, recover out-of-range results
- Small-result analog computation enables:
 - Lower-energy ADC and/or more analog compute with the same ADC range
 - Up to 5x higher efficiency and 3x higher throughput
 - Without modifying or retraining DNNs!

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