Tanner Andrulis

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I'm a fifth-year Ph.D. student at MIT. My current research area is in the modeling and design of specialized accelerators for machine learning. My work has included novel compute paradigms, including analog, compute-in-memory, optical, and superconducting accelerators. Currently I'm working on tools to optimally scheduling deep neural network workloads onto specialized accelerators and applying these tools to novel and heterogenous systems.

Education

- **Ph.D. Electrical Engineering & Computer Science. Massachusetts Institute of Technology** **2021-2027**
  - Advised by Profs. Joel Emer and Vivienne Sze
- **M.S. Electrical Engineering & Computer Science. Massachusetts Institute of Technology** **2021-2023**
  - 5.0/5.0 GPA
  - Master's Thesis titled "Efficient, Accurate, and Flexible PIM Inference through Adaptable Low-Resolution Arithmetic"
- **B.S Computer Engineering, Purdue University West Lafayette** **2017-2021**
  - 3.97/4.0 GPA, Graduated Summa Cum Laude
- **B.S Mathematics, Purdue University** **2017-2021**
  - 3.97/4.0 GPA, Graduated Summa Cum Laude

Publications

- Soojung Bae, Tanner Andrulis, Vivienne Sze, and Joel S. Emer. "Small-Noise is All You Need: Fast and Precise Estimation of Compute-in-Memory Accuracy Loss", under submission.
- Michael Gilbert, Tanner Andrulis, Vivienne Sze, and Joel S. Emer. "The Turbo-Charged Mapper: Fast and Optimal Mapping for Energy-efficient and Low-latency Accelerator Design", MICRO 2026.
- Tanner Andrulis, Michael Gilbert, Vivienne Sze, and Joel S. Emer. "Fast and Fusiest: A Fast and Optimal Fusing Mapper for Tensor Algebra Accelerators", under submission.
- Michael Gilbert, Tanner Andrulis, Vivienne Sze, and Joel S. Emer. "LoopForest: Exploring an Expanded Fusion Mapspace for Reduced Data Movement and Memory Usage", under submission.
- Tanner Andrulis, Ruicong Chen, Anantha Chandrakasan, Hae-Seung Lee, Joel S. Emer, and Vivienne Sze, "A Fast Architecture-Level Model of Analog-Digital-Converters in Compute-In-Memory Systems", ArXIV
- Tanner Andrulis, Gohar Irfan Chaudhry, Vinith Suriyakumar, Joel S. Emer, and Vivienne Sze, "An Architecture-Level Model of Photonic Deep Neural Network Accelerators", ISPASS 2024
- Tanner Andrulis, Joel S. Emer, and Vivienne Sze, "CiMLoop: A Flexible, Accurate, and Fast Compute-In-Memory Modeling Framework" ISPASS 2024. Best paper award winner.

- Tanner Andrulis, “Efficient, Accurate, and Flexible PIM Inference through Adaptable Low-Resolution Arithmetic!” MIT Master’s Thesis, 2023

- Tanner Andrulis, Joel S. Emer, and Vivienne Sze, “RAELLA: Reforming the Arithmetic for Efficient, Low-Resolution, and Low-Loss Analog PIM: No Retraining Required!” ISCA 2023

- Tanner Andrulis, Joel S. Emer, and Vivienne Sze, “Architectural Evaluation of Processing-In-Memory Systems” ASPLOS YArch’ Workshop, 2022

Research Experience

- **Optimal mapping of deep neural network workloads on hardware** **2024-Present**
  - Developing algorithms that can find optimal ways to map deep neural network workloads onto hardware, a problem previously thought intractable.
  - Exploring novel mapsapces

- **Architecture design for superconducting accelerators** **2024-Present**

- **Analog/Digital Compute-In-Memory Accelerator Design & Modeling** **2021-Present**
  - Developing full-stack simulation tools for compute-in-memory accelerators of tensor algebra and deep neural network workloads.
  - Released open-source tools modeling analog devices and compute-in-memory arrays.
  - Enabling co-design and fast design space exploration for these architectures.

- **On-Chip Interconnect Interference Modeling** **2019-2021**
  - Advised by Professor Cheng Kok Koh, Purdue University.
  - Developed computationally-efficient models of inductive/capacitive interference in on-chip interconnects.
  - Lowered the computational complexity bound from $O(N^2)$ to $O(N)$ for accurate simulation of N-wire systems.

- **Purdue VIP Smart Cities Autonomous Drone Research** **2018-2019**
  - Advised by Professor Mohammad Reza Jahanshahi, Purdue University.
  - Developed simulators to test autonomous drone piloting algorithms.
  - Using this infrastructure, explored Reinforcement Learning algorithms to operate building-scanning drones.

Work Experience

- **PhD Research Intern, Nvidia Circuits Research Group** **May-August 2024**
  - Developed tools that automatically optimize how deep neural networks are programmed onto accelerators.
  - Developed a method to find optimal DRAM-access-minimizing programs.

- **Digital Hardware Intern, Qualcomm Technologies, Incorporated** **May-August 2020**
  - Worked with the digital design infrastructure team to develop processor-memory interface systems.
  - Developed tools to automate digital design processes for processor-memory interface systems.

- **Software and Controls Intern, Eaton Corporation** **May-August 2019**
  - Developed diagnostic software and automating scripts to improve testing process of semi-truck control software.

- Authored tools for retrieval of memory contents and diagnosis of errors in semi-truck computer memory.

Teaching Experience

- **Graduate Teaching Assistant, MIT 6.5930 Hardware Architectures for Deep Learning** **2024-2025**

- **Undergraduate Teaching Assistant, Purdue ECE 50863-EDX Computer Network Systems January-May 2021**
  - Led the design of new student programming projects based on cutting-edge computer network research.
  - Tested and modified student assignments for online instruction.
  - Designed systems to support Internet Systems Lab research. Implemented lightweight methods to enable transmission and sharing of flows over multiple tunnels in software-defined networks.

Service

- **Program committee member:** HPCA 2026, MICRO2026
- **Reviewer:** TCASAI 2026, CAL 2026, CAL 2025

Selected Awards

- **Samsung Semiconductor Fellowship** **2023**
- **MIT Siebels Scholar Fellowship** **2022**
- **MIT Irwin Mark Jacobs and Joan Klein Jacobs Presidential Fellow** **2021**
- **Purdue Undergraduate Excellence Award** **2021**
  - Awarded for contributions in creating the ECE-50863 EDX Course.
- **Purdue Fessenden Trott Scholarship** **2017-2021**
- **Purdue Presidential Scholarship** **2017-2021**

Activities

- **MIT Rock Climbing Team** **2021-2023**
- **MIT GSB Organizer** **2021-Present**
  - Social event organizer for the MIT Computer Science & Artificial Intelligence Laboratory (CSAIL).
- **MIT Edgerton House Board Member and Resources Chair** **2021-2023**
- **Purdue IEEE Remote Operated Vehicle Team** **2029-2021**
  - Designed control algorithms for autonomous submarine thruster systems. Enabled submarine to do a backflip for the first time in competition.
  - Developed computer vision algorithms that enabled autonomous submarine to recognize and react to underwater objects.
- **Purdue IEEE Aerial Robotics Team** **2018-2019**
  - Lead designer of collision-avoidance algorithms to pilot autonomous planes between skyscrapers.